REMARKS

Claims 1-13 and 20 are pending. By this amendment, claims 1 and 5 are amended in accordance with the Examiner's suggestions to correct noted informalities. These amendments are not made to overcome prior art, and thus no surrender of claim scope is intended. Applicants submit that the above amendments and added claims do not add new matter to the application and are fully supported by the specification. Applicants respectfully request reconsideration and timely withdrawal of the pending objections and rejections for the reasons discussed below.

Allowable Subject Matter

Applicants appreciate that claim 20 is allowed. Applicants further appreciate that claims 5 and 9-11 contain allowable subject matter.

Regarding claim 20, Applicants agree with the Examiner that the combination of the cited prior art references does not teach or suggest forming a polysilicon layer on the n-type transistor and the p-type transistor, such that the polysilicon layer on the p-type transistor has a shorter height than the polysilicon layer on the n-type transistor. However, Applicants submit that Krivokapic teaches depositing additional polysilicon onto each transistor and etching the added polysilicon, which is not heated, and does not react with the gate polysilicon. Applicants further submit that Kim teaches thermally oxidizing portions of the gate polysilicon and substrate between the gates to form insulation regions, which reduce stress in the areas between the gates. Kim does not teach, nor is it inherent, creating a reaction with polysilicon to create compressive stress in the channel region. Consequently, claim 20 is further distinguishable over the prior art

of record as much for each of these individual features as it is for the distinguishable feature noted by the Examiner.

Regarding claims 5 and 9-11, many of the Examiner's reasons for allowability are correct. However, some statements are not accurate. For example, despite the Examiner's assertions, claims 9 and 10 do not recite "reducing the compressive stresses along a longitudinal direction of the p-type transistor by selective etching the polysilicon layer over both the p-type and n-type transistors." The claimed invention forms compressive mechanical stresses along a longitudinal direction of a channel of the p-type transistor. Additionally, the Examiner states that Krivokapic *et. al.* at col. 5, lns. 19-22 teaches etching the gate polysilicon of the p-type transistor. Instead, this passage teaches depositing a layer of polysilicon over both the n-type and p-type transistor, and then etching the deposited layer of polysilicon back to the top surface of the gate polysilicon. Such steps do not disclose or suggest etching the gate polysilicon of the p-type transistor, as claimed.

Although claims 5 and 9-11 contain allowable subject matter for at least the reasons mentioned above, Applicants decline to amend these dependent claims into independent format because Applicants believe that the base claim (claim 1) recites one or more features not taught or suggested by the prior art. Identification and description of these one or more features is set forth below.

Objection to Drawings

In the Office Action, the drawings were objected to as not including the reference numeral "32" mentioned in the written description. Applicants respectfully decline to provide

corrected drawing sheets at this time because reference numeral 32 is clearly shown in Figure 2D. Accordingly, Applicants respectfully request withdrawal of the drawing objection.

Objection to Claims

In the Office Action, Claim 1 was objected to as not providing proper antecedent basis for "the polysilicon of a gate of the p-type transistor" recited in line 8. The preamble of claim 1 is amended to provide proper antecedent basis, and Applicants respectfully request withdrawal of this objection.

Claim 5 was objected to because the abbreviation "HF" was recited instead of "Hf". Claim 5 is amended to recite "Hf", and withdrawal of the objection of claim 5 is respectfully requested.

The amendments mentioned above are made for the sole purpose of correction, and not for the purpose of avoiding prior art or narrowing the claimed invention. Thus, no change in claim scope is intended, and Applicants do not intend to relinquish any subject matter by these amendments. Applicants respectfully submit that claims 1 and 5, as amended, overcome the stated objection, and respectfully request withdrawal of the objection of claims 1, 5, and 9-11.

35 U.S.C. § 103 Rejection

Claims 1-4, 6-8, and 12-13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U. S. Patent No. 6,512,273 issued to Krivokapic, *et al.* ("Krivokapic") in view of U. S. Patent No. 5,677,232 issued to Kim, *et al.* ("Kim"). This rejection is respectfully traversed.

In order to reject a claim under 35 U.S.C. §103(a), the MPEP mandates that three basic criteria must be met to provide a *prima facie* case of obviousness:

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Claims 1-4, 6-8, and 12-13

The Examiner suggests that the combination of Krivokapic and Kim discloses each of the features recited in claim 1, but this does not appear to be accurate. Specifically, Krivokapic does not teach etching a portion of the polysilicon from the gate of the p-type transistor. Instead, Krivokapic specifically teaches forming polysilicon gates 10, covering the polysilicon gates 10 with an oxide layer 18, forming disposable nitride spacers 20 about the n-type transistor, forming permanent nitride spacers about the p-type transistor, and forming polysilicon spacers 33 about each of the n-type and the p-type transistor such that the top portion of the gate polysilicon 10 is exposed. In other words, once formed, Krivokapic's polysilicon gates 10 are not etched, although other materials, such as oxide, nitride, and additional polysilicon (for spacers 33) are. For example, such materials are deposited and etched back to the top surface of the polysilicon gates 10. (*See*, col. 4, lns 55-56 – "...depositing 500-700 A nitride, then etching back to the top gate surfaces leaving nitride spacers."; and col. 5, lns. 19-21 – "...polysilicon is deposited, then etched back to form polysilicon spacers 22..."). These and other similar passages directly contradict the Examiner's assertions that Krivokapic teaches etching a polysilicon gate, as

recited in claim 1. In fact, etching the polysilicon gate of the p-type transistor as claimed specifically distinguishes over Krivokapic because such etching produces a p-type transistor that has a shorter polysilicon gate than the n-type transistor. For these reasons, claim 1 is allowable over the cited reference.

Claim 1 further recites "...depositing a low resistance material on the p-type transistor and n-type transistor", something not taught by Krivokapic. Applicant's specification teaches at page 7, paragraph 26, that the claimed "low resistance material" is a metal or low-resistance material, such as, for example, Co, Hf, Mo, Ni, Pd_2, Ta, Ti, W and Zr. Thus, in the claimed invention, the low resistance material would not be the polysilicon disclosed in Krivokapic's step 50 or step 80. Consequently, the Examiner's suggestion that Krivokapic's additional deposited polysilicon is a "low resistance material" misapprehends the claimed invention. Additionally, the Examiner admits at page 7, paragraph 2 of the Office Action that "...the prior art does not teach or suggest depositing Co, Hf, Mo, Ni, Pd_2, Ta, Ti, W and Zr on the p-type and n-type transistor...." If Krivokapic does not disclose depositing these materials, and if these materials are each a low resistance material, then Krivokapic, by the Examiner's own admission, fails to disclose or suggest "depositing a low resistance material on the p-type and n-type transistor" as recited in claim 1. Consequently, claim 1 is allowable over the cited reference.

Krivokapic discloses annealing at step 90 to activate various p-channel implants. The Examiner suggests that this disclosure anticipates claim 1, but this appears to be incorrect. Claim 1 recites, in pertinent part:

> ....heating the integrated circuit such that the deposited low resistance material reacts with the polysilicon to form compressive mechanical stresses along a longitudinal direction of a channel of the p-type transistor.

As the Examiner admits, Krivokapic does not disclose depositing a low resistance material. Consequently, it is impossible for Krivokapic to also disclose "heating ... such that the deposited low resistance material reacts with the (gate) polysilicon to form compressive mechanical stresses ..."

Instead, Krivokapic specifically teaches forming tilted channel implants (TCI) (28) beneath the transistor gate after the gate is formed. Contrary to the features of claim 1, TCI injects dopants into the substrate at a predetermined angle to form double-elliptical shapes that extend into the channel region from the edges of the gate and overlap beneath the center of the gate. Consequently, the claimed feature (e.g., heating the integrated circuit such that the deposited low resistance material reacts with the polysilicon to form compressive mechanical stresses along a longitudinal direction of a channel of the p-type transistor) is not disclosed by Krivokapic.

The Examiner suggests that adding Kim cures Krivokapic's deficiencies, but this appears to be incorrect because Kim also does not teach or suggest depositing a low resistance material on the p-type transistor and n-type transistor. Instead, Kim teaches thermally oxidizing exposed portion of the substrate (21) between the sidewall spacers (27) along with top portions of polysilicon mesas (25) to form first insulation regions (29a) between the mesas, and second insulation regions (29b) on the mesas (25). Although Kim discloses compressive stress generally at col. 4, lines 50-60, Kim specifically teaches that using polysilicon for the mesas (25) (instead of the conventional silicon nitride) relieves stress occurring at the interface of the first insulation regions (29a) and the substrate (21), thus reducing the probability of crystal defects in these

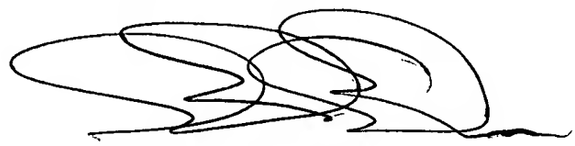
regions. This is not recited in claim 1, which recites heating the integrated circuit such that the deposited low resistance material reacts with the gate polysilicon *to form compressive mechanical stresses* along a longitudinal direction of the channel of the p-type transistor.

The Examiner has failed to establish a *prima facie* case of obviousness because claim 1 recites at least one feature not taught or suggested by the combination of Kapokavic and Kim. Thus, claim 1 is allowable. Claims 3-4, 6-8, and 12-13 are also allowable based on their dependencies from allowable base claim 1. Accordingly, withdrawal of the rejection of claims 1-4, 6-8, and 12-13 is respectfully requested.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to **IBM Deposit Account No. 09-0458** (Fishkill).

Respectfully submitted,



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